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TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

EXAMINER	
MOE, AUNG SOE	
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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/862,523
Filing Date: May 22, 2001
Appellant(s): CLYNES ET AL.

Alan K. Stewart
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 4/21/2006 appealing from the Office action mailed 9/9/2005.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

1,045,578	Chen et al.	10-2000
6,002,433	Watanabe et al	12-1999

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 3-11, 17-18 and 20 are rejected under 35 U.S.C. 102(a) as being anticipated by Chen et al. (EP 1,045,578 A2).

Regarding claim 1, Chen '578 discloses a method of pixel filtering for CMOS imagers (Figs. 1 & 2; col. 4, lines 35+), comprising: scanning each of a plurality of pixels within a block (i.e., noted the pixel block as shown in Fig. 4a-4c; col. 7, lines 10+); designating a pixel as a process pixel (i.e., noted the B pixels as shown in Figs. 3a-4c; see col. 7, lines 10+), the process pixel having adjacent pixels (i.e., noted the A and C pixels as shown in Figs. 3a-4c; see col. 7, lines 10), the process pixel having a process pixel value (i.e., noted the pixel value of the middle pixel B as shown in Figs. 3a-4c; see col. 7, lines 10+), each of the adjacent pixels having an adjacent pixel value (i.e., noted the pixel values of the adjacent pixels A and B as shown in Figs. 3a-4c; see col. 7, lines 1+); and comparing the process pixel value to at least one adjacent pixel value (i.e., col. 6, lines 30+, col. 7, lines 1+, col. 8, lines 5+); and detecting a lowest pixel value

among the adjacent pixels (i.e., as shown in Figs. 3a-3j, the lowest pixel values of the adjacent pixels A and C are respectively determined by the imaging logic 8; see col. 6, lines 30+, col. 7, lines 10+ and col. 8, lines 5+ and col. 9, lines 45+).

Regarding claim 3, Chen '578 discloses wherein comparing compares the process pixel value to a lowest pixel value (as shown in Figs. 3a-3j, the defective-pixel filter 34 of the imaging logic 8 compared the lowest pixel value of the adjacent pixels A/C with the middle pixels B; see col. 8, lines 1+ and col. 9, lines 15+).

Regarding claim 4, Chen '578 discloses further comprising resetting the process pixel to a new pixel value (i.e., as discussed in col. 9, lines 45+, that if the condition of the pixel values are determined to be as shown in Figs. 3g and 3j, then the process pixel B is reset, e.g., replaced, by a new pixel value $B_{corrected}$; see col. 9, lines 45+).

Regarding claim 5, Chen '578 discloses wherein the new pixel value is the average pixel value of the adjacent pixel values (i.e., col. 9, lines 50+).

Regarding claim 6, Chen '578 discloses further comprising detecting a highest pixel value among the adjacent pixels (i.e., noted the pixel values of pixel 54 as shown in Figs. 3g and 3j).

Regarding claim 7, Chen '578 discloses wherein comparing compares the process pixel value to a highest pixel value (i.e., noted form Figs. 3a-3j and 5 that the defective-pixel filter 34 of the imaging logic 8 compared the highest pixel value of the adjacent pixels A/C with the middle pixels B; see col. 8, lines 1+ and col. 9, lines 15+).

Regarding claim 8, Chen '578 discloses further comprising resetting (i.e., Replacing the pixel value B with a new pixel value $B_{corrected}$; see col. 9, lines 45+) the process pixel value (i.e., the B pixel value as shown in Fig. 3j) when the process pixel value is a predetermined value (i.e., noted the value as shown in Fig. 3j) lower than the lowest pixel value (noted form Fig. 3j, a predetermined value is lower than the lowest pixel value A, then the pixel value B is replaced with a new pixel value $B_{corrected}$; see col. 9, lines 45+).

Regarding claim 9, Chen '578 discloses further comprising resetting the process pixel value (i.e., Replacing the pixel value B with a new pixel value $B_{corrected}$; see col. 9, lines 45+) when the process pixel value is a predetermined value (i.e., noted the value as shown in Fig. 3g) greater than the highest pixel value (noted form Fig. 3g, a predetermined value is greater than the highest pixel value C, then the pixel value B is replaced with a new pixel value $B_{corrected}$; see col. 9, lines 45+).

Regarding claim 10, Chen '578 discloses further comprising exposing an array to a light source so as to cast an image on the array (Fig. 1, the sensor array 6; col. 5, lines 20+), the array having at least one block (i.e., noted the block as shown in Fig. 4).

Regarding claim 11, Chen '578 discloses wherein the array is generally grid-shaped (i.e., noted that an array of CMOS sensor cells contain a matrix of pixel array generally formed as a grid-shape).

Regarding claim 17, Chen '578 discloses a method of on-chip pixel filtering for CMOS imagers (Figs. 1 & 2; col. 4, lines 35+), comprising:

scanning each of a plurality of pixels within a block for a pixel value (i.e., see Figs. 3a-4c; col. 7, lines 5+); loading a pixel value into a register (Fig. 5; col. 7, lines 35+ and col. 8, lines 5+); using filter logic (34) to designate a pixel as a process pixel (i.e., noted that the pixel B is designated by the filter logic 34 as a process pixel; see col. 6, lines 30+), the process pixel having adjacent pixels (i.e., noted the pixels A and C as shown in Fig. 3a-4c), the process pixel having a process pixel value (i.e., noted the process pixel values of pixel B as shown in Figs. 3a-3j), each of the adjacent pixels having an adjacent pixel value (i.e., noted the pixel values of the adjacent pixels A and B as shown in Figs. 3a-4c; see col. 7, lines 1+); and using filter logic (34) to compare the process pixel value to at least one adjacent pixel value;

wherein the filter logic (34) compares the process pixel value (i.e., the middle pixel value B as shown in Figs. 3g and 3j) to a lowest pixel value (i.e., noted the lowest pixel value is determined to have a shorter bar as shown in Figs. 3g and 3j), further comprising: detecting the lowest pixel value among the adjacent pixels (i.e., noted from Figs. 3a-3j, the lowest pixel values are determined by the filter logic 34 and the system controller 28); and resetting the process pixel value to a new process pixel value (i.e., Replacing the pixel value B with a new pixel value $B_{corrected}$; see col. 9, lines 45+) when the process pixel value is a predetermined value (i.e., noted the value as shown in Fig. 3j) lower than the lowest pixel value (noted form Fig. 3j, a predetermined value is lower than the lowest pixel value A, then the pixel value B is replaced with a new pixel value $B_{corrected}$; see col. 9, lines 45+).

Regarding claim 18, Chen '578 discloses wherein the filter logic compares the process pixel value to a highest pixel value, further comprising: detecting the highest pixel value among the adjacent pixels; and resetting the process pixel value to a new process pixel value when the

process pixel value is a predetermined value higher than the highest pixel value (i.e., Fig. 5; col. 6, lines 30+, col. 7, lines 1+, col. 8, lines 5+).

Regarding claim 20, Chen '578 discloses wherein the new process pixel value is the average pixel value of the adjacent pixel values (i.e., see col. 9, lines 45+).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen '578 in view of Watanabe et al. (U.S. 6,002,433).

Regarding claims 12 and 13, it is noted although Chen '578 shows the use of block of sensor (i.e., see Figs. 4a and 6), Chen '578 does not explicitly state that the block is generally grid-shaped and has nine pixels as required by the present claimed invention.

However, the above-mentioned clamed limitations are well known in the art as evidenced by Watanabe '433. In particular, Watanabe '433 teaches the use of block of nine pixels arranged in grid-shaped for detection of defective pixel with high precision (i.e., see Fig. 8; col. 1, lines 30-35 and col. 2, lines 55-60) in the imaging system.

In view of the above, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify the system of Chen '578 as taught by Watanabe '433 so that detection of defective pixel can be carried out at high speed with high precision as suggested by Watanabe '433 (i.e., see col. 16, lines 5+).

(10) Response to Argument

I. Appellant's arguments filed on 4/21/2006 have been fully considered but they are not persuasive.

In page 7 of the brief, the Appellant alleged European Paten Application EP 1,045,578 compares a primary pixel to adjacent pixels, but does not **compare adjacent pixels to each other to determine a lowest pixel value among the adjacent pixels**.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., ***compare adjacent pixels to each other*** **to determine a lowest pixel value among the adjacent pixels**) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

In this case, the present claimed inventions merely stated "comparing the process pixel value to at least one adjacent pixel value; and detecting a lowest pixel value among the adjacent pixel" as recited in claim 1, and "the filter logic compares the process pixel value to a lowest pixel value, further comprising: detecting the lowest pixel value among the adjacent pixels" as recited in claim 17, and such limitations are clearly shown by Chen '578.

In particular, Chen '578 clearly discloses that the process pixel value (i.e., noted the B pixels as shown in Figs.3a-4c: see col. 7, lines 10+) is designated by the filter logic (i.e., the elements 8 as shown in Figs. 1, 2 and 5), and comparing the process pixel value (B) to at least one adjacent pixel value having a lowest pixel value (i.e., as shown in Figs. 3i & 3j, the process pixels B is compared with one of the adjacent pixel value A & C having a lowest pixel value, e.g., *the process pixel value "B" is compared to be more than "t" below the lowest adjacent pixel values "A" as shown in Fig. 3j*; see col. 7, lines 5+ and col. 9, lines 35-45).

Moreover, Chen '578 clearly shown, e.g., in Figs. 3a-3j, how to determine/detect the lowest pixel value among the adjacent pixels. For example, it is clear form Figs. 3a-3j of Chen '578 that one of the pixel value among the adjacent pixels is considered to be the lowest pixel value, and this is further evidenced by Chen '578 as discussed in col. 6, lines 30+ and col. 9, lines 35+. In particular, Chen '578 stated in col. 6, lines 30+ that in FIG 3a, the pixel B 52 has a luminance value grater than that of the pixel A 50 and the pixel C 54 has a luminance value greater than that of the pixel B 52, and this clearly implied that the pixel value of "A 50" is determined to be the lowest among the adjacent pixels "B 52" and "C 54" (i.e., as discussed in col. 9, lines 35-45, the logic 34 as shown in Fig. 5 detected the lowest pixel value of "A" among the adjacent pixels B, and C).

Therefore, the Examiner asserts that Chen '578 does in fact anticipated the present claimed invention for at least the reasons discussed above.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

6/23/06

Aung S. Moe

Primary Examiner (2618)

Conferees:

Edward Urban (SPE 2618)

Matthew D. Anderson (SPE 2618)